High Efficiency Step-Up LED Driver with Dual Output LCD Bias Power

Features

- Wide input range: 3.0V~5.5V
- Low quiescent current
- Drive up to 10 series LEDs or 2 parallel strings of 8 series LEDs
  - Backlight efficiency: up to 86%
  - Integrated 40V Power MOSFET
  - Flexible dimming control
    - 256-step I^2C Controlled or
    - High resolution PWM 5~100kHz
  - High accuracy across full load range
  - Programmable LED open-circuit (OVP)/Short protection
  - Low 200mV feedback voltage
  - Internal over voltage protection (default 36V)
- Programmable dual Bias output regulator based on single inductor solution
  - Charge pump PFM mode at light load
  - LCD Bias efficiency: up to 90%
  - Wide dual output voltage range
    - +/-4.0V to +/-6.3V (100mV/step)
  - +/-1.5% V_{POS}/V_{NEG} output voltage accuracy
  - Maximum peak output current up to 80mA
  - Active output discharge function
  - Cycle-by-cycle inductor current limit
- 1 µA shutdown current
- Pb-free Package: WLCSP-18
- -40°C to +85°C Temperature Range

Applications

- Smartphone/Tablet Backlight
- Netbook/Notebook Backlight
- PDA/GPS Backlight
- Portable Media Player

Brief Description

The KTZ8850 is a multifunction power management IC combining a high efficiency step-up LED driver with dual output LCD bias power regulator. It features a versatile constant current LED driver with a high efficiency DC-DC step up “boost” converter architecture. The low-side 40V power MOSFET is integrated in the device, minimizing the total number of external components. Unique technology and high 1.3A current limit allow KTZ8850 to drive up to 36V output (single string of 10 LEDs in series or 2 parallel strings of 8 LEDs in series).

The optimized 1.1MHz switching frequency results in small external component size. The driver is equipped with an internal decoder that allows digital FB control dimming for 256-step (8-bit) current programming and can be used for dimming via I^2C interface.

High resolution PWM dimming control is also included for extended dimming range. For power savings, the PWM pin can be used for Content Adaptive Brightness Control (CABC) schemes.

Various protection features are built into the KTZ8850, including cycle-by-cycle input current limit protection, LED open-circuit (output over voltage) protection and thermal shutdown protection. The leakage current in shutdown mode is less than 1µA.

An LDO and a charge pump generate dual outputs at +5V (default) and -5V (default), whose voltages can be programmed via an I^2C interface. By integrating synchronous rectification MOSFETs for the step-up converter and charge pump, the KTZ8850 maximizes conversion efficiency up to 90%.

The device integrates compensation and soft-start circuitry, which results in a simpler and smaller solution with much fewer external components. High switching frequency (2.2MHz) allows the use of a smaller inductor and capacitor to further reduce the solution size.

The I^2C-compatible interface controls the dual output voltages and accesses the programmable functions and registers on the device.

KTZ8850 is available in a RoHS compliant 18-ball 2.47 x 1.27mm WLCSP package.

Typical Application

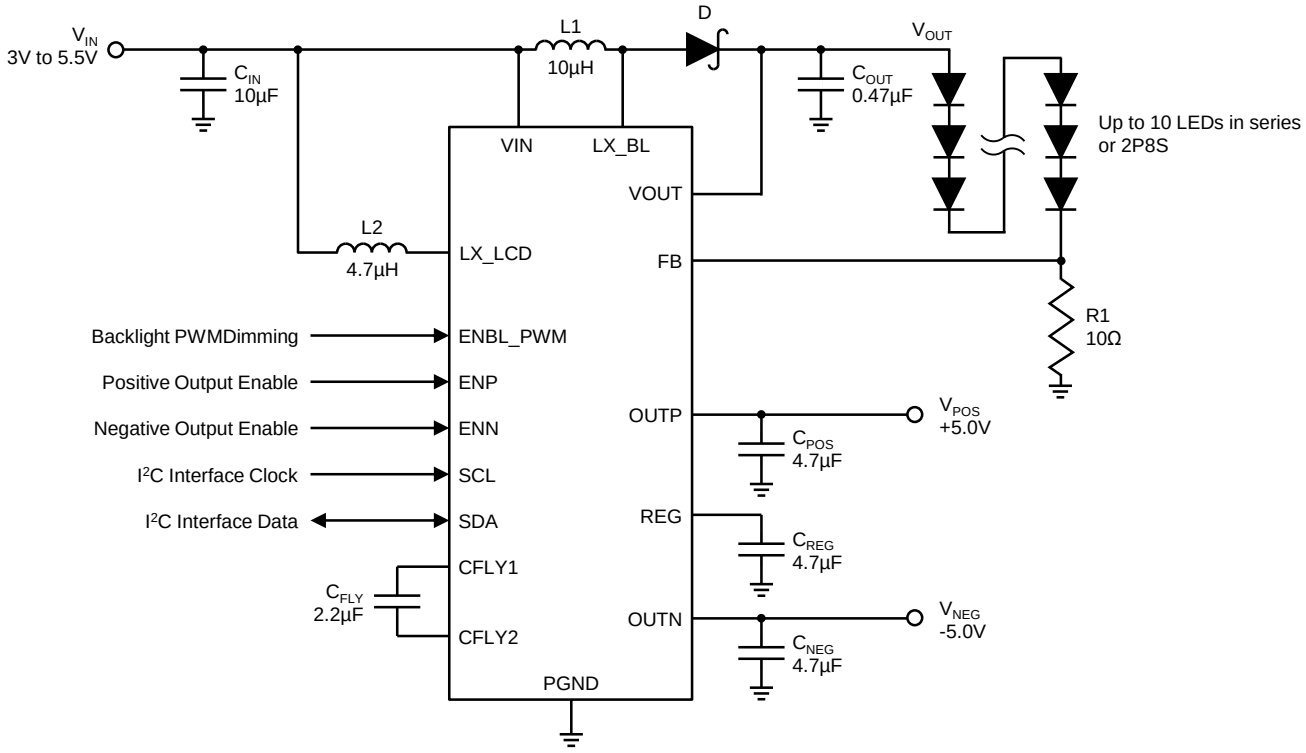
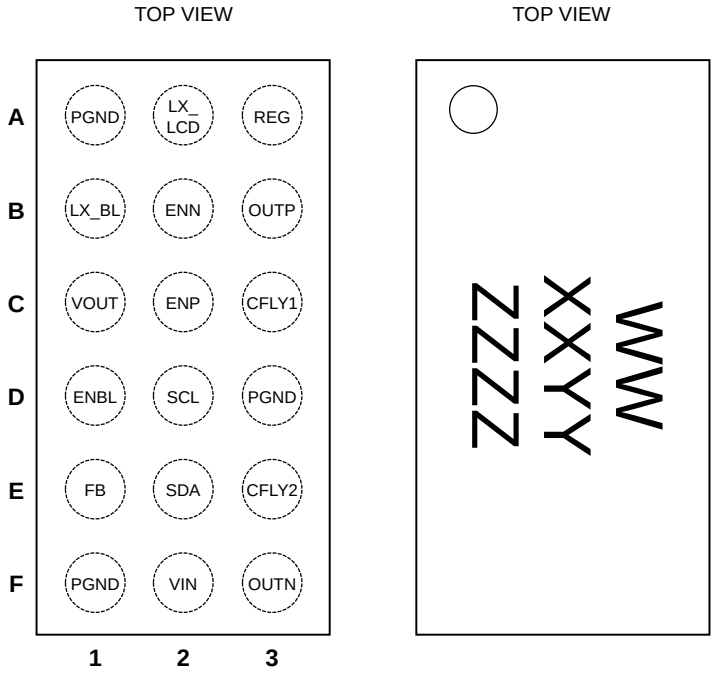


Figure 1. Typical Application Circuit for I²C Interface Control

Pin Descriptions

Pin #	Name	Function
A1, D3, F1	PGND	Power Ground pin. All GND pins must be connected in the PCB for proper operation.
A2	LX_LCD	Switching node of the bias step-up converter
A3	REG	Bias step up converter output pin
B1	LX_BL	Switch node pin of backlight step up dc-dc converter
B2	ENN	Enable pin for negative power (OUTN). There is an internal 500kΩ pull-down resistor at this pin.
B3	OUTP	LDO output pin of the positive power
C1	VOUT	Backlight output voltage sense pin
C2	ENP	Enable pin for positive power (OUTP). There is an internal 500kΩ pull-down resistor at this pin.
C3	CFLY1	Negative charge pump flying capacitor pin
D1	ENBL_PWM	Pulse width controlled dimming input. Connect this pin to VIN to enable I^2C control. There is an internal 400kΩ pull-down resistor at this pin.
D2	SCL	Clock of the I^2C interface.
E1	FB	Backlight feedback voltage pin
E2	SDA	Data of the I^2C interface.
E3	CFLY2	Negative charge pump flying capacitor pin
F2	VIN	Input supply pin for the IC
F3	OUTN	Charge pump output pin of the negative power

WLCSP-18



18-Bump 2.47mm x 1.27mm x 0.6mm

Top Mark
WW = Device ID Code,
XX = Date Code, YY = Assembly Code,
ZZZZ = Serial Number

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
VIN	Input voltage	-0.3 to 7	V
LX_BL	High voltage nodes	-0.3 to 44	V
VOUT	Output Voltage pin	-0.3 to 44	V
FB, SCL, SDA,	Control pins	-0.3 to VIN+0.3	V
LX_LCD, CFLY1	High voltage nodes and charge pump voltage	-0.3 to 7	V
OUTP, REG	Output voltage pin	-0.3 to 7	V
OUTN, CFLY2	Output voltage pin and charge pump voltage	-7 to 0.3	V
ENP, ENN, ENBL_PWM	Control pins	-0.3 to VIN+0.3	V
T_J	Junction Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Capabilities

Symbol	Description	Value	Units
WLCSP-18, 2.47mm x 1.27mm			
θ_{JA}	Thermal Resistance – Junction to Ambient[2]	70	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$	1.64	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-8.7	mW/°C

Ordering Information

Part Number	Marking	Operating Temperature	Package	Functions	
				Backlight	Dual Output
KTZ8850EUC-TR	JFXXYYZZZZ[3]	-40°C to +85°C	WLCSP-18	1P10S/2P8S	±5V (default)

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time

2. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an 2s2p PCB .

3. XX = Date Code, YY = Assembly Code, ZZZZ = Serial Number.

Electrical Characteristics[4]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of –40°C to +85°C, while *Typ* values are specified at room temperature (25°C). VIN = 3.6V,

Symbol	Description	Conditions	Min	Typ	Max	Units
IC Supply						
V_{IN}	Input operating range		3.0		5.5	V
UVLO	Input under voltage lockout	Rising edge		2.5	2.65	V
$UVLO_{HYST}$	UVLO hysteresis			0.15		V
I_Q	IC standby current	Not switching ENP = ENN = ENBL_PWM = V_{IN}		1.5		mA
	IC operating current	Switching ENP = ENN = ENBL_PWM = V_{IN}		2.1		mA
I_{SHDN}	Shutdown current[5]	ENP = ENN = ENBL_PWM = 0V			1	µA
Step-Up Converter for LED Backlight						
V_{FB}	FB pin accuracy		184	200	216	mV
V_{FB_DATA}	FB pin accuracy	Reg 04 data = 25	14.3	20.3	26.3	mV
I_{FB}	FB pin bias current				0.1	µA
$R_{DS(ON)}$	NMOS on-resistance			0.6		Ω
I_{LX}	LX pin leakage current			1.0		µA
I_{LIM}	Peak NMOS current limit			1.3		A
$I_{INRUSH-SU}$	Peak Inductor Current During Startup	V_{IN} = 3.6V, L = 10µH, 10 LEDs, I_{LED} = 20mA, C_{OUT} = 0.47µF		400		mA
$I_{INRUSH-OL}$	Peak Inductor Current During Open-Load Condition	V_{IN} = 3.6V, L = 10µH, C_{OUT} = 0.47µF, V_{OVP} = 36V		450		mA
F_{SW}	Oscillator frequency			1.1		MHz
D_{max}	Maximum duty cycle		92	95		%
V_{OV}	Over voltage threshold (Default)	Measured at V_{OUT} pin		36.5		V
T_S	Start-up time			3		msec
Step-Up Converter for LCD Bias Power						
I_{LIM}	Peak NMOS current limit		0.8			A
F_{SW}	Oscillator frequency			2.2		MHz
D_{max}	Maximum duty cycle		80	86		%
T_S	Start-up time			0.7		msec
OUTP - Positive Output, V_{POS}						
V_{POS}	Positive output voltage range		4.0		6.3	V
V_{POS_ACC}	Positive output voltage accuracy	T_A = -40°C to +85°C	-1.5		+1.5	%
I_{LIM_POS}	Positive output current limit		200			mA
V_{DROP}	Dropout voltage	I_{OUT} = 50mA		50		mV
V_{LINE}	Line regulation	ΔV_{OUT} = 1V, I_{OUT} = 30mA		0.06		%/V
V_{LOAD}	Load regulation	ΔI_{OUT} = 50mA		11		mV
$R_{DISCHARGE}$	Discharge resistance			70		Ω

4. KTZ8850 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

5. KTZ8850 I^2C inputs are disabled when both ENP and ENN are low.

Electrical Characteristics[6]

Symbol	Description	Conditions	Min	Typ	Max	Units
OUTN - Negative Output, V_{NEG}						
V_{NEG}	Negative output voltage range		-4.0		-6.3	V
V_{NEG_ACC}	Negative output voltage accuracy	T_A = -40°C to +85°C	-1.5		+1.5	%
I_{LIM_NEG}	Negative output max regulated current		80			mA
F_{SW_CP}	Charge pump switching frequency			1.1		MHz
V_{LINE}	Line regulation	ΔV_{OUT} = 1V, I_{OUT} = 30mA		0.02		%/V
V_{LOAD}	Load regulation	ΔI_{OUT} = 50mA		6.3		mV
$R_{DISCHARGE}$	Discharge resistance			20		Ω
Logic Control; ENBL_PWM for backlight						
V_{TH-L}	ENBL_PWM logic low threshold				0.4	V
V_{TH-H}	ENBL_PWM logic high threshold		1.4			V
R_{CTRL}	ENBL_PWM pull down resistor			300		kΩ
t_{off}	ENBL_PWM pulse width to shutdown	CTRL high to low	2.5			ms
f_{DIM}	Recommended PWM dimming frequency		5		100	kHz
D_{DIM}	PWM dimming duty cycle resolution	f_{DIM} = 20kHz	1			%
		f_{DM} = 30kHz	1			%
Logic Control; ENP, ENN						
V_{TH-L}	ENP, ENN pin logic low threshold	V_{IN} = 3.0V to 5.5V			0.4	V
V_{TH-H}	ENP, ENN pin logic high threshold		1.4			V
R_{ENP}	ENP pull down resistor			500		kΩ
R_{ENN}	ENN pull down resistor			500		kΩ
I^2C-Compatible Voltage Specifications (SCL, SDA)						
V_{IL}	Input Logic Low Threshold	SDA, SCL			0.4	V
V_{IH}	Input Logic High Threshold	SDA, SCL	1.2			V

6. KTZ8850 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics[7]

Symbol	Description	Conditions	Min	Typ	Max	Units
I²C-Compatible Timing Specifications (SCL, SDA)[8] see *Figure 2*						
t_1	SCL (Clock Period)		2.5			µsec
t_2	Data In Setup Time to SCL High		100			nsec
t_3	Data Out Stable After SCL Low		0			nsec
t_4	SDA Low Setup Time to SCL Low (Start)		100			nsec
t_5	SDA High Hold Time After SCL High (Stop)		100			nsec
f_{SCLK}	SCL Clock Frequency				400	KHz
t_{BUF}	Bus Free Time Between a STOP and START Condition		1.3			µsec
t_{HD_STA}	Hold Time (Repeated) START Condition		0.6			µsec
t_{LOW}	LOW Period of SCL Clock		1.3			µsec
t_{HIGH}	HIGH Period of SCL Clock		0.6			µsec
t_{HD_DAT}	Data Hold Time9		0		0.9	µsec
t_{SU_DTA}	Data Setup Time[8]		100			nsec
t_R	Rise Time of Both SDA and SCL Signals				300	nsec
t_F	Fall Time of Both SDA and SCL Signals				300	nsec
t_{SU_STO}	Setup Time for STOP Condition		0.6			µsec
Thermal Shutdown						
TJ_{-TH}	IC junction thermal shutdown threshold			140		°C
	IC junction thermal shutdown hysteresis			15		°C

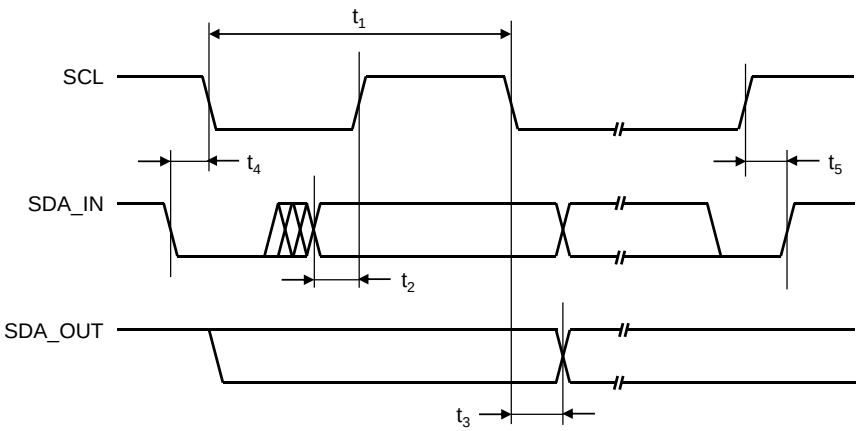


Figure 2. I²C Compatible Interface Timing

7. KTZ8850 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

8. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the VIHMIN of the SCL signal) to bridge the undefined region of the falling edge of SCL.

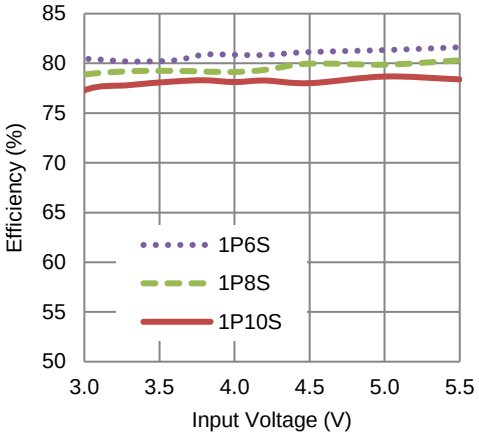
9. A fast-mode device can be used in a standard-mode system, but the requirement t_{SU_DAT} = to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + t_{SU_DAT} = 1000 + 250 = 1250nsec before the SCL line is released.

Typical Characteristics

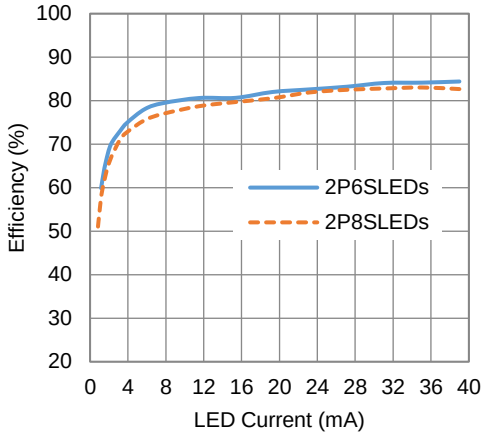
LED Backlight

V_{IN} = 3.6V, L1 = 10µH (LQH3NPN100MJRL), C_{IN} = 10µF, C_{OUT} = 0.47µF, with 8 LEDs in series at 20mA, T_A = 25°C, unless otherwise specified. ENN and ENP are OFF.

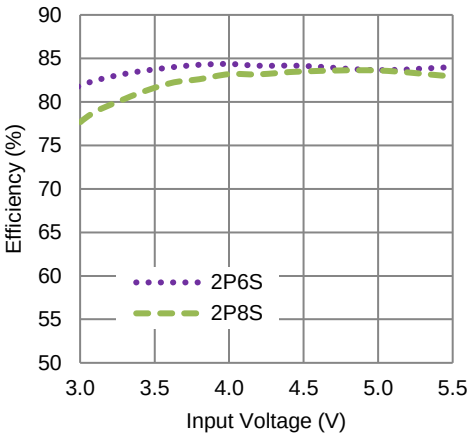
Efficiency vs Input Voltage



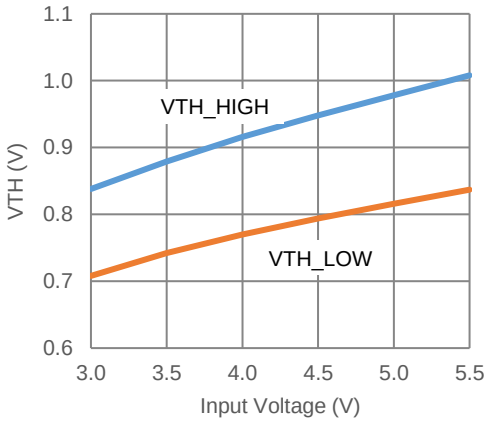
Efficiency vs. LED Current per string



Efficiency vs. Input Voltage
(I_{OUT} = 40mA, 2P6S LEDs)



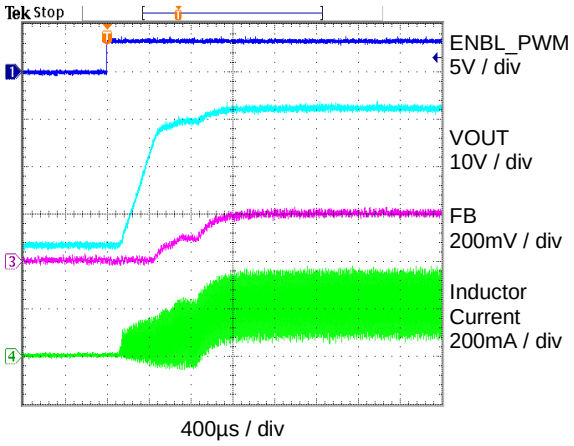
ENBL_PWM Logic Threshold Voltage



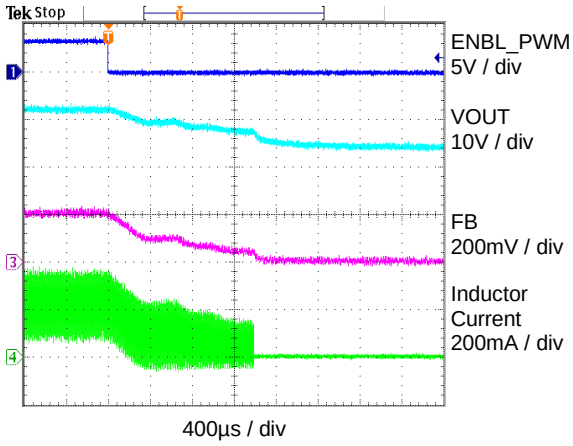
Typical Characteristics

V_{IN} = 3.6V, L1 = 10µH (LQH3NPN100MJRL), C_{IN} = 10µF, C_{OUT} = 0.47µF, with 8 LEDs in series at 20mA, T_A = 25˚C, unless otherwise specified. ENN and ENP are OFF.

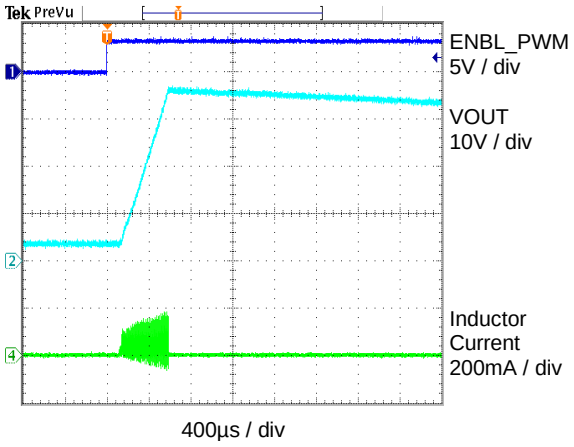
Soft Start Turn On



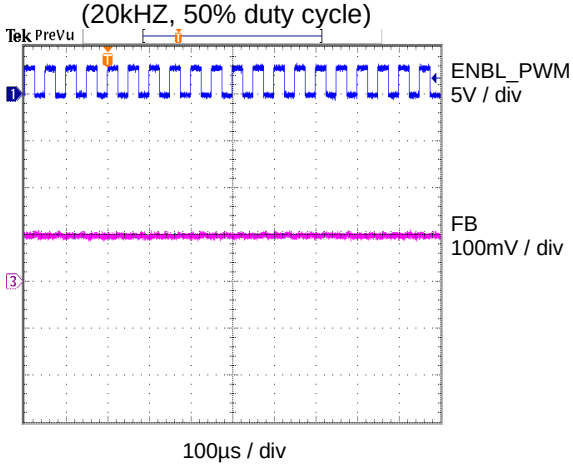
Turn Off



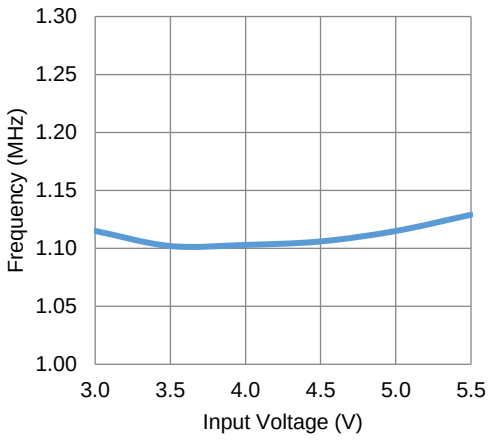
Turn On with LED Open (OVP)



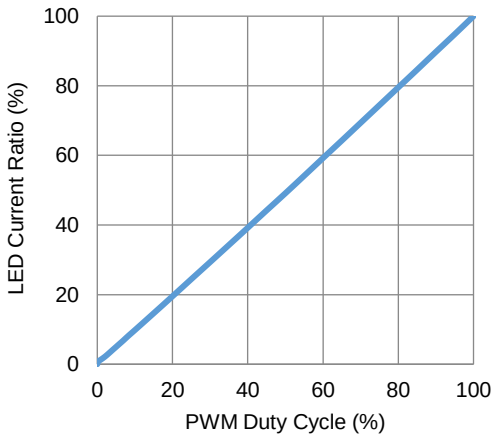
PWM Dimming
(20kHZ, 50% duty cycle)



Backlight Switching Frequency



PWM Dimming Linearity (20kHz)

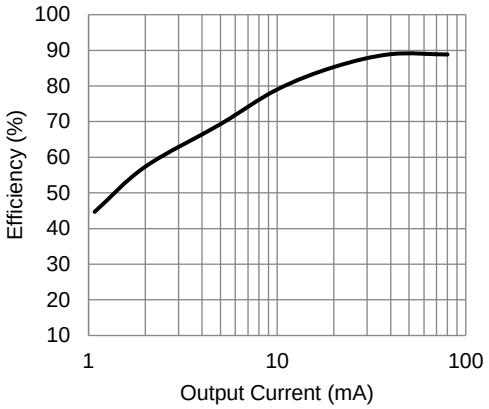


Typical Characteristics

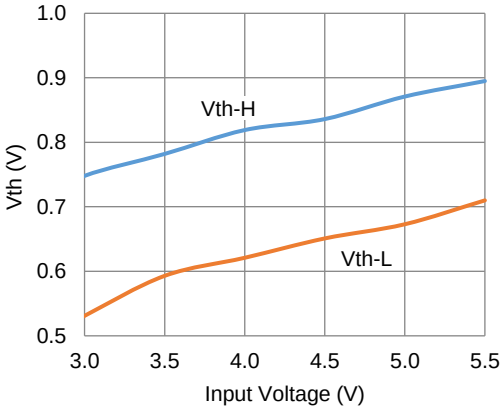
LCD Bias

V_{IN} = 3.7V, L2 = 4.7µH (LQH3NPN4R7MJRL), C_{IN} = C_{REG} = C_{POS} = C_{NEG} = 4.7µF, C_{FLY} = 2.2µF, I_{POS} = -I_{NEG} = 40mA, T_A = 25°C, unless otherwise specified. Default setting V_{POS}/V_{NEG} = ±5.0V, V_{REG} Offset = 200mV.

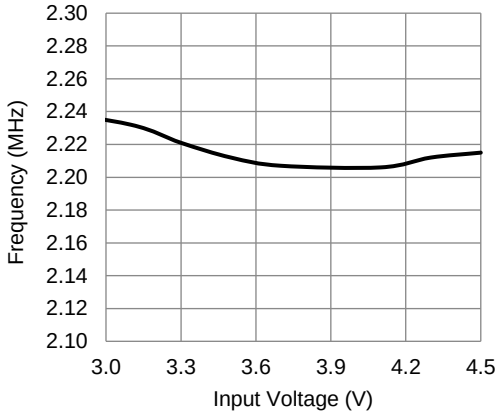
Efficiency vs. Output Current



ENP/ENN Logic Threshold Voltage



Step-Up Converter Switching Frequency



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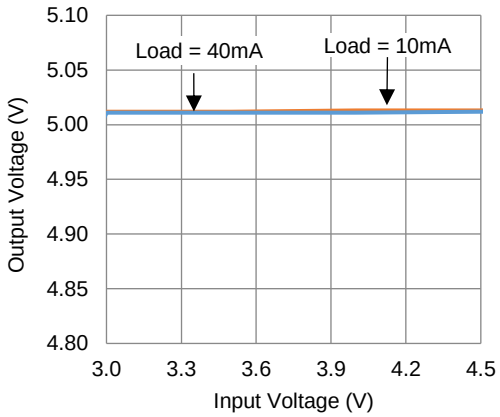
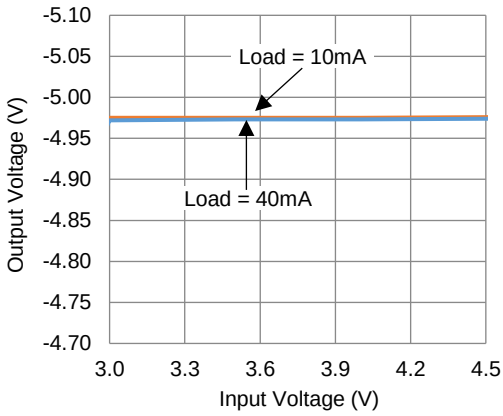
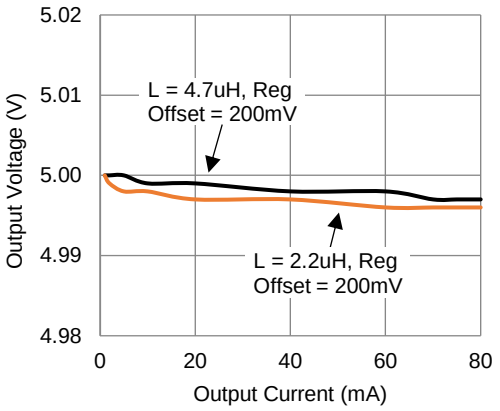
OUTP Line Regulation



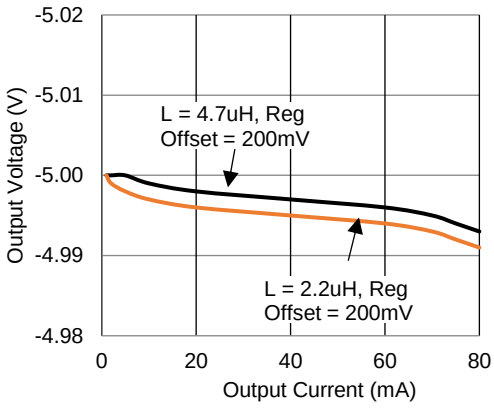
OUTN Line Regulation



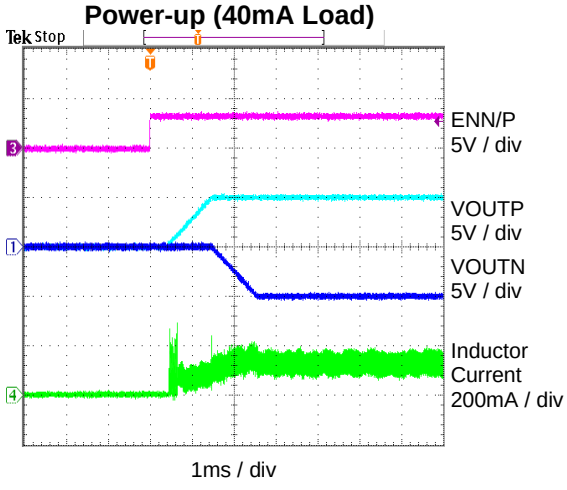
OUTP Load Regulation



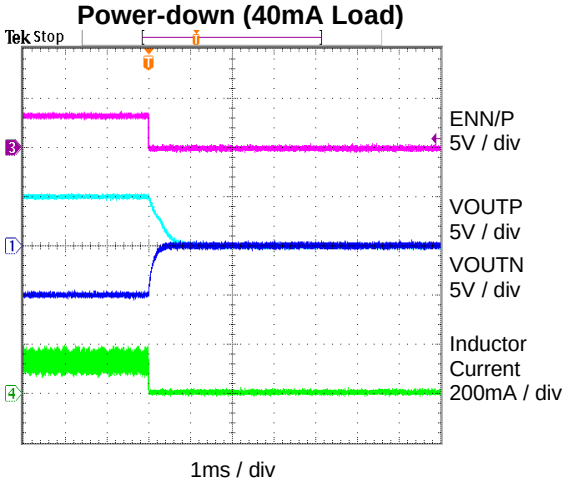
OUTN Load Regulation



Power-up (40mA Load)



Power-down (40mA Load)



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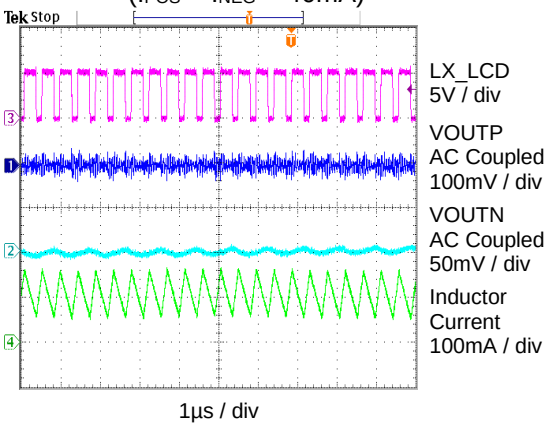
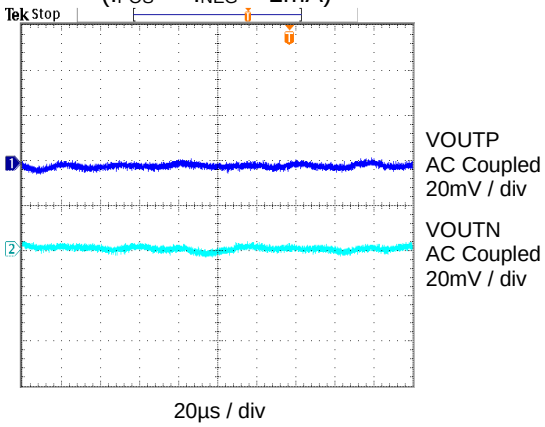
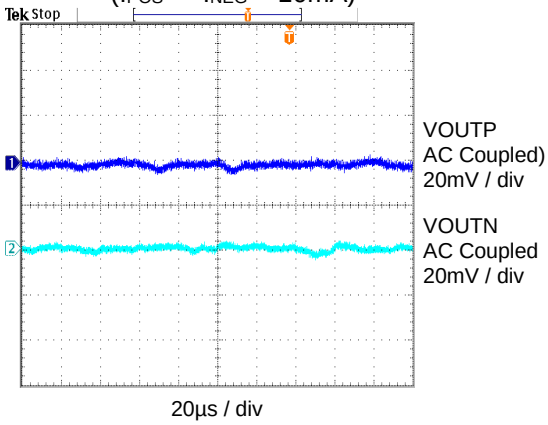
Switching Waveform
(I_{POS} = I_{NEG} = 40mA)



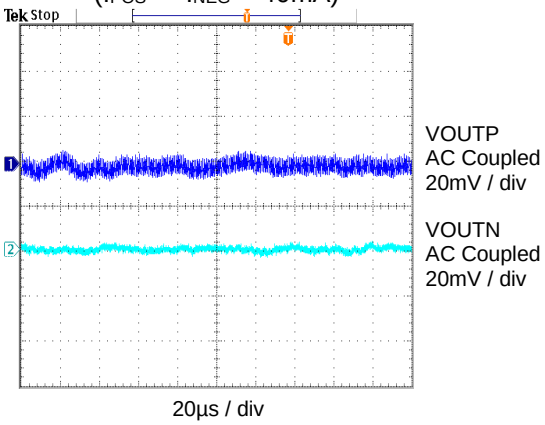
Steady-state Operation
(I_{POS} = -I_{NEG} = 1mA)



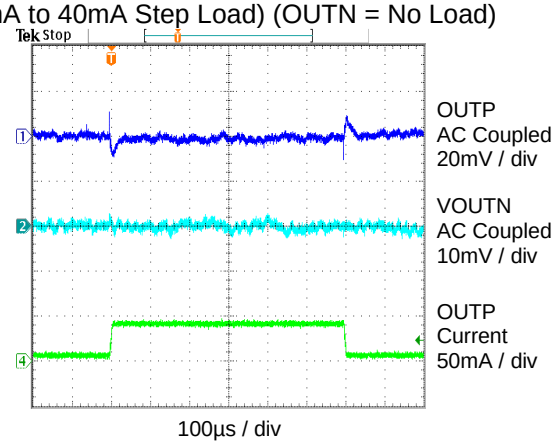
Steady-state Operation
(I_{POS} = -I_{NEG} = 10mA)



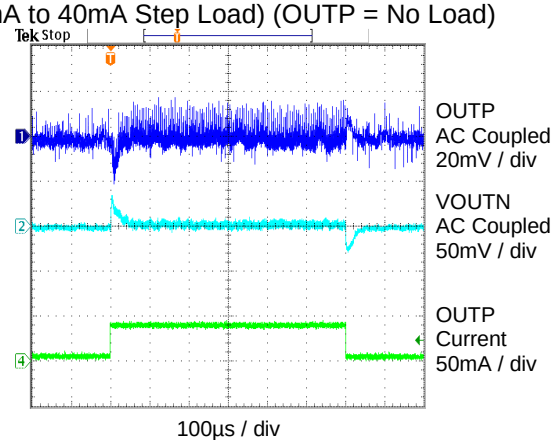
Steady-state Operation
(I_{POS} = -I_{NEG} = 40mA)



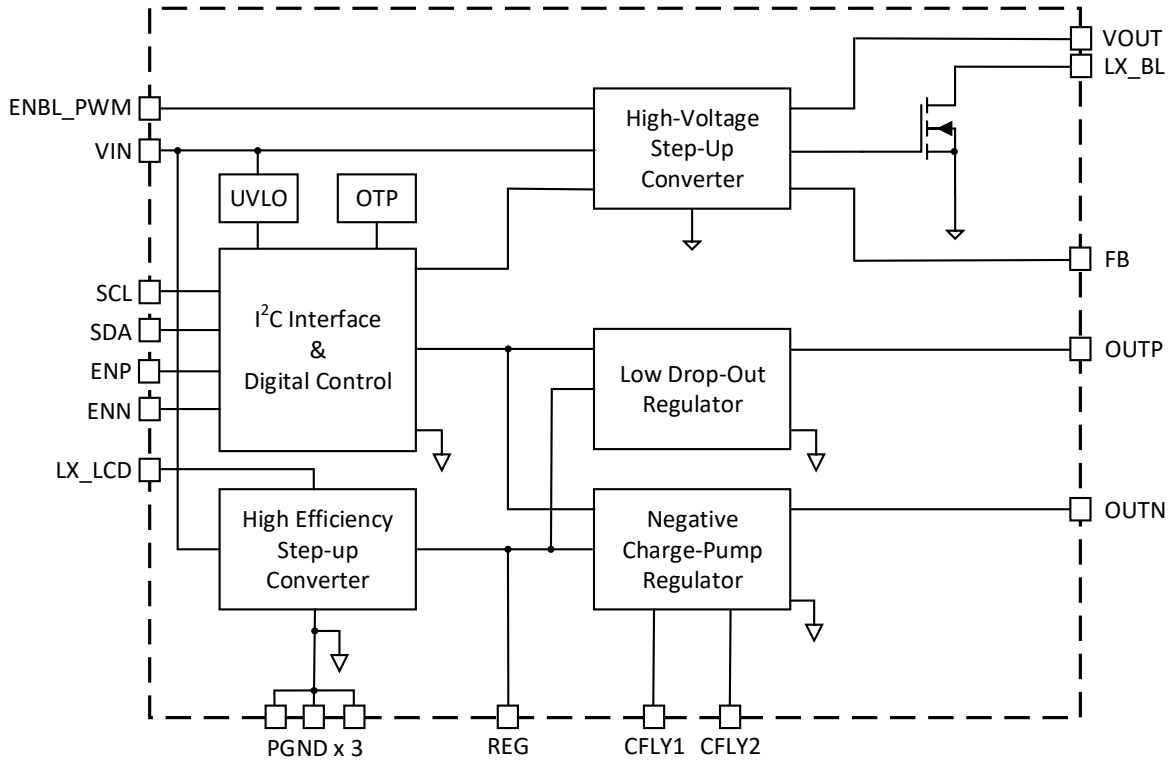
Load Transient
(5mA to 40mA Step Load) (OUTN = No Load)



Load Transient
(5mA to 40mA Step Load) (OUTP = No Load)



Functional Block Diagram



Functional Description

The KTZ8850 is a high efficiency step-up LED driver and dual output LCD bias power regulator. The LED driver uses a constant-frequency current-mode boost converter architecture to control the LED current by regulating the feedback voltage. At the beginning of each switching cycle, the internal power MOSFET turns on between the LX_BL node and GND. A slope compensation ramp is added to the output of the current sense amplifier and the result is fed into the positive input of the comparator. When this voltage goes above the output voltage of the error amplifier, the power MOSFET is turned off. The voltage at the output of the error amplifier block amplifies the difference between the reference voltage and the feedback voltage (FB), so that FB voltage can be regulated to the reference voltage.

The backlight driver has built-in soft-start to limit the inrush current during startup and to limit the amount of overshoot on the output. Protection features in the KTZ8850 include over-voltage protection (OVP), cycle-by-cycle current limit protection and thermal shutdown. OVP protects in the event where an LED fails open, which forces the feedback voltage to zero. This causes the boost converter to operate in maximum duty cycle mode, ramping up the output voltage. Switching will stop when the output reaches the OVP threshold. The OVP feature protects the IC from damaging itself by exceeding the voltage rating on LX_BL/VOUT pins. The OVP threshold voltage is programmable with a default at 36.5V.

The ENBL_PWM pin can be used for either PWM dimming or to enable I^2C backlight dimming. In PWM dimming mode, PWM pulses are provided at the ENBL_PWM pin to program the reference voltage (FB) according to the duty cycle of the PWM signal, so that the LED current is proportional to the PWM duty cycle. The simplest control method is accomplished by toggling ENBL_PWM between high and low to program the output current between I_{MAX} and 0mA. I_{MAX} is set by the resistor R1 connected between FB and GND.

$$I_{MAX} = V_{FB\_MAX} / R1$$

To control the backlight current via I²C, Reg4 should be programmed with data to program the reference voltage, thereby modulating the LED current. The data contains 8 bits, yielding 256 different current levels.

The KTZ8850 contains a dual switching converter to generate both a positive and a negative power supplies that are required by TFT-LCD display panels. The KTZ8850 integrates a boost regulator, LDO and charge pump, to generate two output rails from +4.0V to +6.3V for positive output voltage and from -4.0V to -6.3V for negative output voltage programmable via I²C interface. The synchronous boost converter generates a positive voltage that is regulated down by an integrated LDO, providing the positive supply rail (OUTP). The negative supply rail (OUTN) is generated by an integrated negative charge pump driven from the boost converter output pin REG. The operating mode can be selected between smartphone and tablet in order to get the best efficiency possible based on the application. The device topology allows to draw 100% asymmetrical currents on each output in regards to the other output.

Under Voltage Lockout (UVLO)

The device is enabled once the voltage on VIN pin exceeds the UVLO threshold of 2.5 V maximum. No output voltage will however be generated as long as the enable signals are not pulled high. The device, as well as all converters (step-up converter, LDO, charge pump), are disabled as soon as the VIN voltage falls below the UVLO falling threshold. This guarantees a proper operation even in the event of important line transients when the battery gets suddenly heavily loaded.

A short delay starts as soon as VIN rises above the UVLO threshold to prevent the device from turning on after an unwanted VIN voltage spike. Once this delay has passed, the output rails can be enabled and disabled as desired with the enable signals without any delay.

Active Discharge

The positive rail OUTP and the negative rail OUTN can be actively discharged by KTZ8850. The output discharge settings can be programmed by the I²C interface; the default value is ON. When the supply output is powered down, KTZ8850 will discharge the corresponding output(s) through the associated $R_{DISCHARGE}$ resistor connected to ground. The power-down happens when both enable signals (ENN, ENP) go logic low.

Step Up DC-DC Converter Operation for Bias

The synchronous step up converter uses a current mode topology and operates at a quasi-fixed frequency of typically 2.2MHz, allowing chip inductors such as 2.2µH or 4.7µH to be used. The converter is internally compensated and provides a regulated output voltage automatically adjusted depending on the programmed OUTP (positive) and OUTN (negative) voltages.

Step Up DC-DC Converter Power-Up and Soft-Start for Bias

The boost converter starts switching as soon as the either enable signal, ENN or ENP, is pulled high and that the voltage on VIN pin is above the UVLO (under voltage lockout) threshold. If the enable signal is already high when VIN reaches the UVLO threshold, the boost converter starts switching. The boost starts up with an integrated soft-start to avoid excessive inrush current drawn from the battery. The output voltage REG is slowly ramped up to its target value.

Step Up DC-DC Converter Power-Down for Bias

The boost converter stops switching when VIN reaches the UVLO falling threshold or after the last block has been disabled, if VIN is still above the UVLO. For example, due to a special sequencing, the LDO might still be operating while the inverting charge pump is already disabled, in which case, the boost continues operating until the LDO is disabled.

LDO Regulator Operation for Bias

The Low Dropout regulator (or LDO) generates the positive voltage rail OUTP by regulating down the output voltage of the boost converter (V_{REG}). Its inherent PSRR helps filtering the output ripple of the boost converter in order to provide on OUTP pin a clean voltage used as supply for the source driver IC of the display.

LDO Regulator Power-Up and Soft-Start for Bias

The LDO starts operating as soon as the ENP signal is pulled high, and VIN voltage is above the UVLO (under voltage lockout) threshold and that the boost converter has reached its Power Good threshold. In case the enable signal is already high when VIN reaches the UVLO threshold, the boost converter starts first and then

the LDO will start once the boost converter has reached its target voltage. The LDO integrates a soft-start that slowly ramps-up its output voltage VPOS.

LDO Regulator Power-Down and Discharge for Bias

The LDO stops operating when VIN drops below the UVLO threshold minus the hysteresis, or when the ENP is pulled low. The positive rail can be actively discharged to GND during power-down if required. A discharge selection bit is available to enable or disable this function.

LDO Regulator Setting the Output Voltage for Bias

The output voltage of the LDO is programmable via an I^2C compatible interface from 4.0 V to 6.3V via 5-bit with 100mV steps, with an additional 87.5mV via 3-bit control with 12.5mV steps.

Inverting Charge Pump Operation for Bias

The inverting charge pump generates the negative voltage rail OUTN from the output voltage of the boost converter (V_{REG}). The converter uses 4 switches operating and an external flying capacitor to generate the negative rail. Two of the switches are turned on in the first phase to charge the flying capacitor up to VREG, and in the second phase they are turned-off and the two others turn on to pump the energy negatively out of the CFLY capacitors.

Inverting Charge Pump Power-Up and Soft-Start for Bias

The charge pump starts operating as soon as the ENN signal is pulled high, and VIN voltage is above the UVLO (under voltage lockout) threshold and the boost converter has reached its Power Good threshold. If the enable signal is already high when VIN reaches the UVLO threshold, the boost converter will start first and then the charge pump will start once the boost converter has reached its target voltage. The charge pump integrates a soft-start that slowly ramps-up its output voltage OUTN.

Inverting Charge Pump Power-Down and Discharge for Bias

The charge pump stops operating when VIN drops below the UVLO threshold minus the hysteresis or when the ENN is pulled low. The negative rail can be actively discharged to GND during power-down if required. A discharge selection bit is available to enable or disable this function.

Inverting Charge Pump Setting the Output Voltage for Bias

The output voltage of the charge pump is programmable via an I^2C compatible interface from -4.0V to -6.3V via 5-bit with 100mV steps, with an additional -87.5mV via 3-bit control with -12.5mV steps.

Thermal Shutdown

Thermal shutdown feature is included in the KTZ8850. When the IC junction temperature (T_J) reaches 140°C, the IC immediately enters shutdown mode. Once T_J drops 15°C to approximately 125°C, the IC resumes normal operation.

Shutdown Current

When both ENP/ENN inputs are pulled low, KTZ8850 is turned off and the shutdown current is limited to 1µA max. Once the device is in shutdown mode, it no longer responds to I^2C commands. The KTZ8850 must be restarted by transitioning at least one of the enable input, ENP or ENN, from low to high. If the I^2C interface is not used, both SDA and SCL inputs should be tied high (for example to VIN directly) or through pullup resistors. These two inputs should never be left floating (unconnected).

Application Information

I²C Serial Data Bus

The KTZ8850 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. The KTZ8850 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The KTZ8850 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined in Figure 3:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Setup and hold times must also be taken into account.

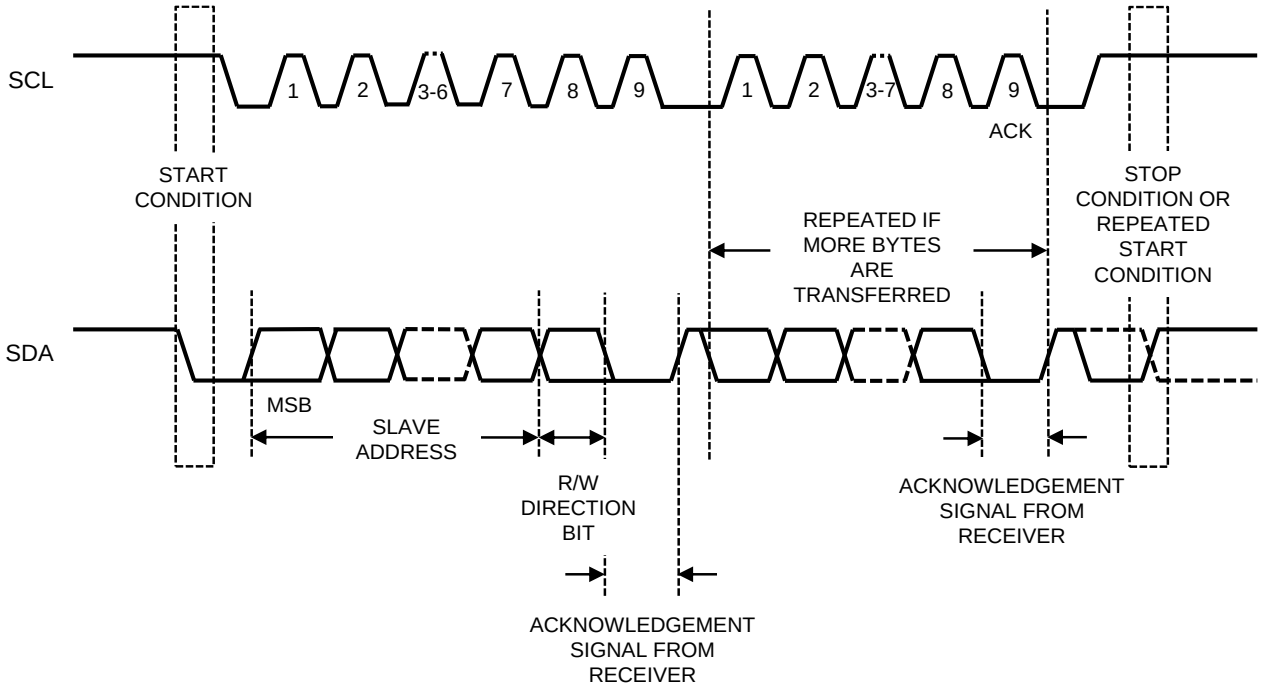


Figure 3. Data Transfer on I2C Serial Bus

The KTZ8850's 7-bit slave device address is 0111110 binary (or 0x3E).

There are two kinds of I2C data transfer cycles: write cycle and read cycle.

I²C Write Cycle

For I²C write cycle, data is transferred from a master to a slave. The first byte transmitted is the 7-bit slave address plus one bit of '0' for write. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first. Figure 4 shows the sequence of the I²C write cycle.

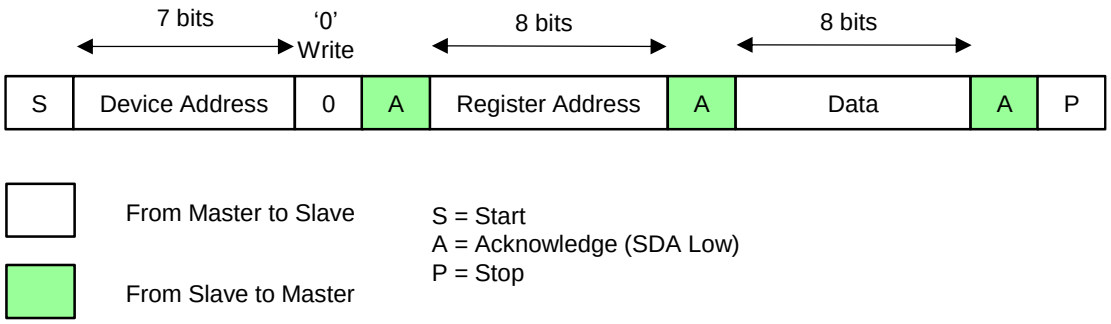


Figure 4. I²C Write Cycle

I²C Write Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (0111110 for KTZ8850) and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master sends 8-bit data for that addressed register.
- Slave sends acknowledge.
- If master sends more data bytes, the register address will be incremented by one after each acknowledge.
- Master generate stop condition to finish the write cycle.

I²C Read Cycle

For I²C read cycle, data is transferred from a slave to a master. But to start the read cycle, master needs to write the register address first to define which register's data to read. Figure 5 shows the steps of the I²C read cycle.

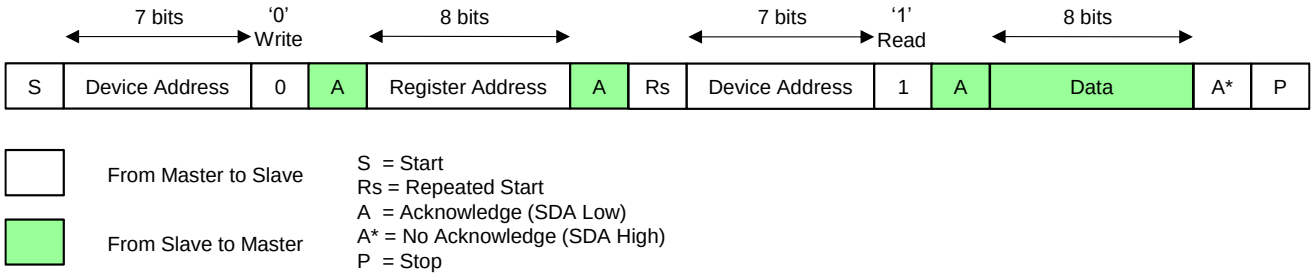


Figure 5. I²C Read Cycle

I²C Read Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (0111110 for KTZ8850) and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master generates repeated start condition.
- Master sends 7-bit slave address (0111110 for KTZ8850) and 1-bit data direction '1' for read.
- Slave sends acknowledge if the slave address is matched.
- Slave sends the data byte of that addressed register.
- If master sends acknowledge, the register address will be incremented by one after each acknowledge and the slave will continue to send the data for the updated addressed register.
- If master sends no acknowledge, the slave will stop sending the data.
- Master generate stop condition to finish the read cycle.

I²C Serial Bus Register Map for Dual Output Bias and LED Backlight Driver

The device has six registers, Reg0 to Reg5. Each register includes one data byte (8 bits) that can be written or read via the I²C interface.

Register Map for Dual Output Bias and LED Backlight Driver

Reg Address	Register Byte [7:0]							
	7	6	5	4	3	2	1	0
Reg 0x00	Set VOUTP Fine [2:0] (12.5mV steps)			Set VOUTP [4:0] (100mV steps from 4V to 6.3V)				
Reg 0x01	Set VOUTN Fine [2:0] (-12.5mV steps)			Set VOUTN [4:0] (-100mV steps from -4V to -6.3V)				
Reg 0x02	Reset Ctrl [2:0]			CP PFM Enable	Ramp Order [1:0]		Ramp Rate [1:0]	
Reg 0x03	Boost Offset [2:0]			BLEN_PWM	Enable [1:0]		Discharge OUTP	Discharge OUTN
Reg 0x04	Backlight [7:0]							
Reg 0x05	<Reserved*>						Backlight OVP [1:0]	

* When writing to the register, always write “0” in the reserved bits.

Register Map Functions and Default Values

Reg#	Register Name	Address (Hex)	Default Value (Hex) (Reset Value)
Reg0	VPOS (positive voltage output) Fine & Coarse Register	00	0A
Reg1	VNEG (negative voltage output) Fine & Coarse Register	01	0A
Reg2	Reset & Control Register	02	00
Reg3	Enable, Discharge & Boost Offset Register	03	43
Reg4	Backlight brightness Register	04	FF
Reg5	Backlight OVP Register	05	00

I²C Register Description

The following tables summarize the settings of each I²C register.

VPOS Positive Voltage Output Setting Register (ADDR 00h, Default 0Ah)

VPOS Voltage Setting 4.0V to 6.3V in 100mV steps, plus additional 87.5mV in 12.5mV steps

VPOS = 4.0V + (code1 * 100mV) + (code2 * 12.5mV).

Table 1. VPOS (positive voltage output) Fine & Coarse Register

Bits [7:5] OUTP Fine Control	Bits [4:0] OUTP Coarse Control
000 = 0mV (Default) 001 = 12.5mV 010 = 25.0mV 011 = 37.5mV 100 = 50.0mV 101 = 62.5mA 110 = 75.0mV 111 = 87.5mV	0 0000 = 4.0V 0 0001 = 4.1V 0 0010 = 4.2V 0 0011 = 4.3V 0 0100 = 4.4V 0 0101 = 4.5V 0 0110 = 4.6V 0 0111 = 4.7V 0 1000 = 4.8V 0 1001 = 4.9V **0 1010 = 5.0V (Default)** 0 1011 = 5.1V 0 1100 = 5.2V 0 1101 = 5.3V 0 1110 = 5.4V 0 1111 = 5.5V 1 0000 = 5.6V 1 0001 = 5.7V 1 0010 = 5.8V 1 0011 = 5.9V 1 0100 = 6.0V 1 0101 = 6.1V 1 0110 = 6.2V 1 0111 = 6.3V

VNEG Negative Voltage Output Setting Register (ADDR 01h, Default 0Ah)

VNEG Voltage Setting -4.0V to -6.3V in -100mV steps, plus additional -87.5mV in -12.5mV steps

VNEG = -4.0V + (code1 * -100mV) + (code2 * -12.5mV).

Table 2. VNEG (negative voltage output) Fine & Coarse Register

Bits [7:5] OUTN Fine Control	Bits [4:0] OUTN Coarse Control
000 = 0mV (Default) 001 = -12.5mV 010 = -25.0mV 011 = -37.5mV 100 = -50.0mV 101 = -62.5mA 110 = -75.0mV 111 = -87.5mV	0 0000 = -4.0V 0 0001 = -4.1V 0 0010 = -4.2V 0 0011 = -4.3V 0 0100 = -4.4V 0 0101 = -4.5V 0 0110 = -4.6V 0 0111 = -4.7V 0 1000 = -4.8V 0 1001 = -4.9V **0 1010 = -5.0V (Default)** 0 1011 = -5.1V 0 1100 = -5.2V 0 1101 = -5.3V 0 1110 = -5.4V 0 1111 = -5.5V 1 0000 = -5.6V 1 0001 = -5.7V 1 0010 = -5.8V 1 0011 = -5.9V 1 0100 = -6.0V 1 0101 = -6.1V 1 0110 = -6.2V 1 0111 = -6.3V

Reset and Bias Control Register (Address 02h, Default 00h)

Reset Control

Register Bits [7:5] controls the reset mode. The five available options are listed in Table 4. It is recommended to reset the chip completely by setting Bits [7:5] = 111.

CP PFM Enable

Enable PFM mode at light load for the charge-pump. Default is OFF (0). For highest efficiency, the charge pump can be operated in PFM mode at low current on negative output. To minimize the output ripple under light load condition, PFM mode should be disabled.

VPOS and VNEG Ramp Order

The output voltage turn-on and turn-off order can also be programmed via I^2C. The default value is 00 and all four startup and shutdown sequences are summarized below,

Table 3. Bias Voltages Ramp Order Options[10]

Ramp Order Options	ENP and ENN transitioned	
Bits [3:2]	**Low to High**	**High to Low**
00	OUTP ramps up to 5V first, then OUTN ramps down to -5V	OUTN ramps up to 0V first, then OUTP ramps down to 0V
01	OUTN ramps down to -5V first, then OUTP ramps up to 5V	Both OUTP and OUTN ramp to 0V together
10	Both OUTP and OUTN ramp to 5V and -5V together	Both OUTP and OUTN ramp to 0V together
11	OUTP ramps up to 5V, and OUTN ramps down to -5V about 2ms after ENP & ENN transitioned	OUTN ramps up to 0V, and OUTP ramps down to 0V about 1ms after ENP & ENN transitioned

VPOS and VNEG Ramp Rate

The soft-start output voltage ramp from 0 to +/- 5V can be set to one of 4 different values. The default value is 1.33ms (00).

Table 4. Reset & Control Register

<table>
<tr><th>Bits [7:5]
Reset Control</th><th>Bit [4]
CP PFM EN</th><th colspan="3">Bits [3:2]
Ramp Order[10]</th><th>Bits [1:0]
Ramp Rate
0 to 5V</th></tr>
<tr><td rowspan="5">0x0 = Do Nothing (Default)
100 = Do nothing (bit 2 cleared)
101 = Reset Main Digital only
110 = Reset Registers only *
111 = Reset Complete Chip *</td><td rowspan="5">0 = Disable (Default)
1 = Enable</td><td></td><td>OFF to ON</td><td>ON to OFF</td><td rowspan="5">00 = 1.33ms (Default)
01 = 0.89ms
10 = 3.55ms
11 = 0.44ms</td></tr>
<tr><td>00 =</td><td>P then N (Default)</td><td>N then P (Default)</td></tr>
<tr><td>01 =</td><td>N then P</td><td>P & N Together</td></tr>
<tr><td>10 =</td><td colspan="2">P & N Together</td></tr>
<tr><td>11 =</td><td>Ramp P then N after delay</td><td>Discharge N then P after delay</td></tr>
</table>

* Both commands “Reset Registers Only” (Bits [7:5] = 110) and “Reset Complete Chip” (Bits [7:5] = 111) will reset SDA to high, which may trigger No-Acknowledge on the I^2C bus. However, all registers or the complete chip is successfully reset once the corresponding code is sent. The I^2C Acknowledge bit functions normally in the next I^2C command.

10. ENN and ENP should be tied together for correct operation

OFFSET, Enable and Discharge Register (ADDR 03h, Default 43h)

REG Offset Control

The REG output node (output of step-up controller) is set to the following value:

$$V_{REG} = Max\ (V_{POS}, V_{NEG}) + V_{OFFSET}$$

V_{REG} default value is the maximum of either (VPOS or -VNEG) + 200mV.

For example, if VPOS = 5.1V and VNEG = -5V, then the default V_{REG} = 5.1V + 0.2V = 5.3V

BL_I²C_Enable

Enables 8-bit control via I²C. Default is OFF (0) allowing PWM brightness control

OUTP & OUTN Enable Control

Turns on bias outputs OUTP & OUTN using I²C. Default is OFF (00).

Note: Turning ON either OUTP or OUTN output also turns-on the boost converter for the REG voltage.

Fast Discharge

Allows quick discharge of OUTP and OUTN nodes when the outputs are disabled. Default is ON (11).

Table 5. Enable, Discharge & Boost Offset Register

Bit [7:5] REG Offset	Bit [4] BL_I2C_Enable	Bit [3:2] Enable	Bit [1] Discharge OUTP	Bit [0] Discharge OUTN
000 = 100mV 001 = 150mV **010 = 200mV (Default)** 011 = 250mV 100 = 300mV 101 = 350mV 110 = 400mV 111 = 450mV	**0 = PWM (Default)** 1 = I²C Enabled	**00 = OFF if ENP & ENN Low (Default)** 01 = Force N ON 10 = Force P ON 11 = Force P & N ON	0 = Disable **1 = Enable (Default)**	0 = Disable **1 = Enable (Default)**

Backlight Control Setting Register (ADDR 04h, Default FFh)

Controls LED brightness by programming the FB voltage in 256 linear steps, as shown below.

VFB (mV) = (Code + 1) x 200 / 256 mV

The minimum value of this register is 04h and the default value is FFh.

The relationship between the LED current and FB voltage is given by the equation:

I_{MAX} = VFB / R1

Table 6. Backlight brightness Register

Bits [7:0] I^2C Backlight Control[11]
00000100 = 3.91mV 00000101 = 4.69mV …… 01111111 = 50mV 10000000 = 50.78mV …… **11111111 = 200mV (Default)**

Table 7. Backlight OVP Register

Bits [7:5]	**Bits [1:0]** Backlight OVP
<Reserved*>	**00 = 36.5V (Default)** 01 = 36.5V 10 = 30.6V 11 = 24.8V

* When writing to the register, always write “0” in the reserved bits.

11. It is recommended not to use codes 00000100 & 00000101 as the accuracy cannot be guaranteed.

LED Maximum Current Setting

The backlight LED maximum current setting, IMAX, is determined by the feedback resistor R1 (connected between FB and GND pins). The feedback voltage is internally set at 200mV at 100% dimming setting. The LED current is programmed according to the formula I_{MAX} = 200mV/R1. For accurate LED current settings, precision 1% resistors are recommended. The formula and table for R1 selection are shown below.

$$R1 = 200mV/I_{MAX}$$

Table 8. Current Setting Resistor (1%Values)

R1 (Ω) 1% Values	IMAX Current (mA)
200	1
40.2	5
20.0	10
13.3	15
10.0	20
6.7	30
2.0	100

PWM Brightness Dimming Control

Backlight LED Brightness can be controlled by driving the ENBL_PWM pin with a PWM signal (5kHz to 100kHz). The relationship between the duty cycle and FB voltage is given by the equation:

$$V_{FB} = DC \times 200mV$$

Where DC is the duty cycle of the PWM signal applied to ENBL_PWM pin, and 200mV is the default internal reference voltage.

The KTZ8850 internally applies the PWM input signal to the 200mV reference voltage which creates a 200mV (peak) signal with the same duty cycle as the PWM input signal. This is fed into an RC low pass filter which gives a DC voltage proportional to the duty cycle of the PWM signal. This voltage is connected to the error amplifier as the reference voltage for the FB pin regulation. This means the PWM signal controls the current via translation to a DC signal to accomplish analog dimming. The advantage of this method is the elimination of audible noise which can occur when the LED current is pulsed at the frequency of the PWM dimming signal. For best performance, the PWM dimming frequency should be in the range of 5kHz to 100kHz.

I²C Brightness Dimming Control

Backlight LED Brightness can also be adjusted by using I²C to program the FB voltage in 256 linear steps. To enable I²C dimming, the ENBL_PWM pin should be high and remain high until the backlight is required to turn off. The default step is full scale when the device is first enabled (V_{FB} = 200 mV). The programmed reference voltage is stored in an internal register. A power reset brings the value back to the default setting; however, using ENBL_PWM to shut down the IC will not reset the internal register. Restarting the IC to I²C dimming mode without setting the new FB voltage value will set the FB voltage back to the previous setting before the IC is shut down by ENBL_PWM pin.

Inductor Selection for Backlight

A 10µH inductor is recommended for the typical application. If high efficiency is a critical requirement, a low DCR inductor should be selected. The inductor saturation current rating should exceed the peak input current.

Table 9. Recommended Inductor Part Numbers

Inductor Part Number	Value (µH)	DCR (Ω)	Saturation Current (A)	Dimensions (mm)	Manufacturer
LQH3NPN100MJRL	10	0.24	0.81	3 x 3 x 1.1	Murata
VLF4014AT-100MR90	10	0.26	0.9	3.5 x 3.7 x 1.4	TDK
LPS4018-103ML	10	0.200 max	1.3	4 x 4 x 1.8	Coilcraft
VLCF5020T-100MR	10	0.182 max	1.13	5 x 5 x 2.0	TDK

Capacitor Selection for Backlight

Small size ceramic capacitors are ideal for KTZ8850 application. A 10µF input capacitor and a 1µF output capacitor are suggested for 10-series LED applications. For high output current applications like 2P8S, larger value output capacitors like 2.2µF are recommended to minimize output ripple.

Table 10. Recommended Ceramic Capacitor Vendors

Manufacturer	Website
Murata	www.murata.com
AVX	www.avx.com
Taiyo Yuden	www.t-yuden.com

Diode Selection for Backlight

The KTZ8850 requires an external diode connected between LX and VOUT. A Schottky diode is recommended because of its low forward voltage drop and fast reverse recovery time. The current rating of the Schottky diode should exceed the peak current of the boost converter. The voltage rating should also exceed the target output voltage.

Table 11. Recommended Schottky Diode Part Numbers

Application	Schottky Diode Part Number	Forward Voltage (V)	Forward Current (mA)	Reverse Voltage (V)	Manufacturer
up to 10 series LEDs	PMEG4010	0.54	1000	40	NXP
4/5/6/8/10-series LEDs, 36V OVP	B150	0.75	1000	50	Vishay

Capacitor Selection for Dual Output Bias

Small size ceramic capacitors with low ESR are ideal for all applications. A 4.7µF input capacitor and a 4.7µF output capacitor at REG are suggested. The voltage rating of these capacitors should exceed the maximum possible voltage at the corresponding pins. The input capacitor should be placed as close as possible to the input pin and the PGND pin of the KTZ8850. For better input voltage filtering, this value can be increased or two capacitors can be used: one 4.7µF input capacitor for the boost converter as well as a 1µF bypass capacitor close to VIN pin. For output capacitors, higher capacitor values can be used to improve the load transient response.

Table 12. Recommended Capacitor Selection

Capacitor	Comments
2.2uF/16V	CFLY
4.7uF/16V	CIN, CPOS, CNEG, CREG
10uF/16V	CNEG, COUT

Manufacturer	Website
Murata	www.murata.com
AVX	www.avx.com
Taiyo Yuden	www.t-yuden.com

Inductor Selection for Dual Output Bias

An inductor in the range of 2.2μH to 10μH with low DCR can be selected for the boost converter. To estimate the inductance required for applications, calculate the maximum input average current as the following

$$I_{IN(MAX)} = \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

Where, η is the converter efficiency and can be approximated as 90% for the typical case. In order to have smaller current ripple (to improve efficiency and minimize output voltage ripple), larger inductance will be required. If inductor ripple current needs to be less than 40% of the average input current, then

$$\Delta I_L = \frac{V_{IN} \cdot D \cdot T_S}{L} \le 40\% \cdot \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

Where duty cycle can be estimated as

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Then

$$\Delta I_L = \frac{V_{IN} \cdot (V_{OUT} - V_{IN}) \cdot T_S}{L \cdot V_{OUT}} \le 40\% \cdot \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

Therefore, the inductance can be calculated as

$$L \ge \frac{V_{IN}^2 \cdot (V_{OUT} - V_{IN}) \cdot \eta}{40\% \cdot V_{OUT}^2 \cdot I_{OUT(MAX)} \cdot f_S}$$

Where, f_S is the switching frequency of the boost converter.

Table 13. Recommended Inductor Part Numbers

Value (µH)	Manufacturer	Inductor Part Number	DCR (Ω)	Saturation Current (A)	EIA Size
2.2	Murata	LQM2HPN2R2MG0	0.08	1.3	1008
4.7	Murata	LQH3NPN4R7MJRL	0.12	1.18	3 x 3 x 1.1mm

Flying Capacitor Selection for Bias

The charge pump needs an external flying capacitor. The minimum value for smartphone application is 2.2µF and 4.7µF for tablet application. Special care must be taken while choosing the flying capacitor as it will directly impact the output voltage accuracy and load regulation performance. Therefore, a minimum capacitance of 1.0µF and 2.2µF respectively is recommended for smartphone and tablet applications. For proper operation, the flying capacitor value must be lower than the output capacitor of the boost converter on VREG pin.

Recommended PCB layout

The high frequency switching operation of KTZ8850 requires careful attention to board layout and component placement in order to maintain stability. The input capacitor should be connected closely to the input pin and the PGND pin of the KTZ8850 so as to optimize the decoupling effect. The charge pump flying capacitor should be connected immediately next to CFLY1 and CFLY2 pins. The path formed by inductor, Schottky diode and output capacitor should be kept as short as possible to minimize noise and ringing.

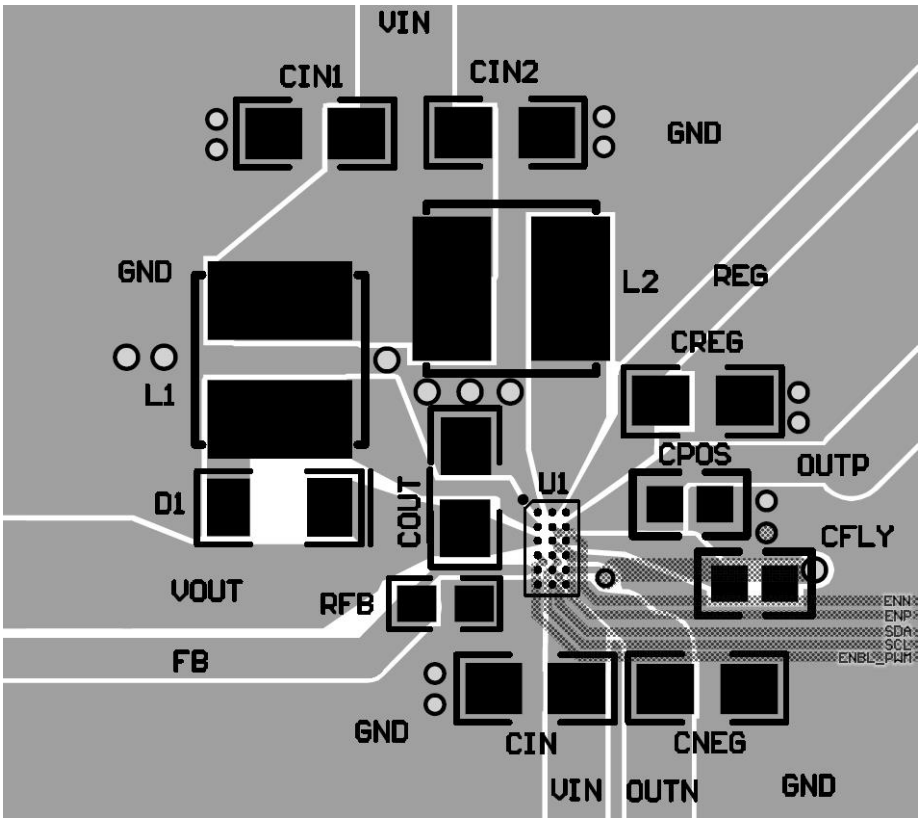
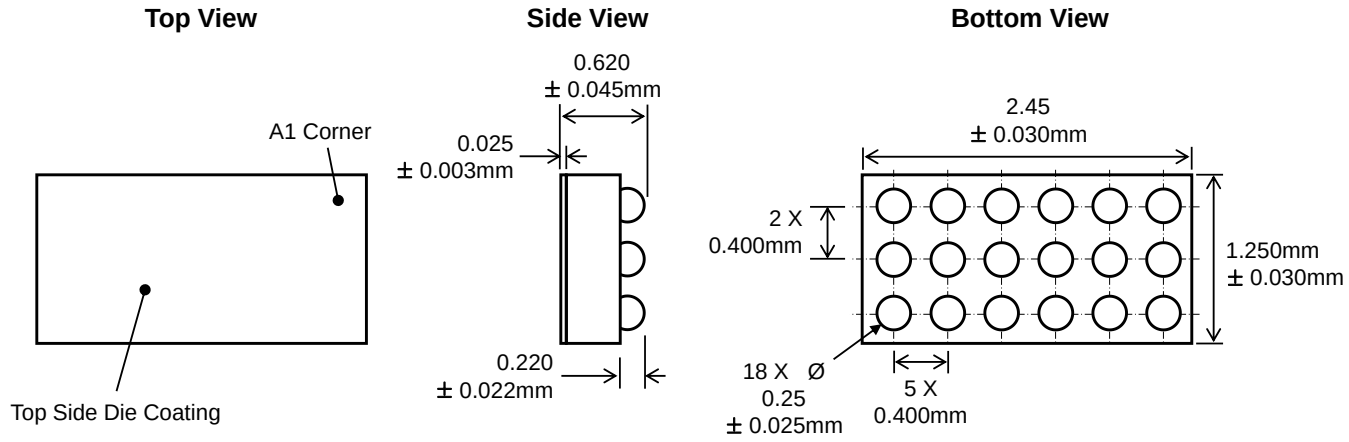


Figure 6. Recommended PCB Layout

Packaging Information

WLCSP-18, 2.47mm x 1.27mm

(Unit: mm)



WLCSP-18-Bump Recommended Land Pattern